High Speed Low Power Flash ADC Design for Ultra Wide Band Applications

SenthilSivakumar M, Banupriya M

Abstract— This paper presents a high speed low power flash ADC design for applications such as radar detection and wide band radio receivers. The flash ADC architecture consists of a sample and hold circuit, preamplifier, comparator and digital decoder to perform a high speed operation. The analog signal is converted to digital signal and is amplified with high operating frequency. The track and latch based design help to generate the full scale digital signal. The output signal is then taken through the digital decoder. The result is obtained by using Tanner EDA with 1.8v, 0.18µm TSMC technology file and the results were also verified using the theoretical formula. The design has obtained the power of 5.3mW/ 2.5µsec, propagation delay of 0.62nsec.

Index Terms— Charge injection, Clock feed through, Digital decoder, Fast override recovery, Flash ADC (Analog to Digital Converter), Kickback noise, Preamplifier, Sample and Hold (S/H), Track and latch, Trans-conductance, UWB (ultra Wide Band).

1 Introduction

The usual method of analog input to a microprocessor is to use an ADC. An ADC accepts an analog input, a voltage or a current, and converts it to a digital word that can be read by a microprocessor. The flash ADC is the fastest type available [1], which is used in wireless communication [7], ultra pulse signal generation, optical communication link, radar detection and ultra wide band receivers [4] & [5].

A flash ADC has one comparator per voltage step [1]. A 4-bit ADC will have 16 comparators; an 8-bit ADC will have 256 comparators. One input of all the comparators is connected to the input to be measured. The other input of each comparator is connected to one point in a string of resistors [8]. As you move up the resistor string, each comparator trips at a higher voltage. All of the comparator outputs connect to a block of logic that determines the output based on which comparators are low and which are high.

The conversion speed of the flash ADC is the sum of the comparators delay and the logic delay (the logic delay is usually negligible). Flash ADCs are very fast, but take enormous amounts of IC real estate to implement. Because of the number of comparators required, they tend to be power hogs, drawing significant current [6]. A 10-bit flash ADC IC may use half an ampere.

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2 Structure of Flash ADC

Flash ADC is constructed by a group of (2^N-1) comparators that can compare the signals generated by sample and hold circuit with different reference voltages [2]. The comparator will generate a digital thermometer code as an output value. These digital thermometer code outputs are converted as an n-bit binary number system using a decoder. In this paper we introduce a new architecture for flash ADC which consist of sample and hold circuit, preamplifier section, latch-track comparator and digital decoder. The function of sample and hold circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. The preamplifier amplifies the input signal to improve the comparator sensitivity and isolate the input to the comparator. The function of latch-track comparator [3] is to compare the voltage at one of its inputs against the voltage at other input and extremely amplifies their difference in the track level. Digital decoder generates the n-bit binary output from the output of comparator thermometer code. Figure 1 shows the structure of Flash ADC. Each stage is discussed in detail below:-

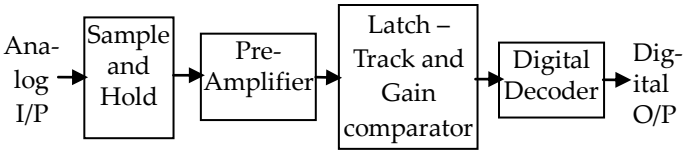

Fig 1: Structure of Flash ADC

2.1 Sample and Hold

Sample and hold (S/H) is an important analog building block with many applications including analog to digital converter (ADC) and switch capacitor filters. The function of this circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Normally Flash ADC is processed directly by 2^n-1 comparator, so it does not need sample and hold circuit. But an inclusion of

sample and hold circuit in front of Flash ADC improves the dynamic performance of ADC. Unfortunately, in reality the performance of ideal sample and hold circuit is poor because of the following two major errors, charge injection and clock feed through.

The fraction k, of the channel charge that is injected into Characteristics is given by equation,

$$\Delta Q_{ch} = kQ_{ch} = -kWLC_{ox}(V_{DD} - V_{th} - V_{in}) \quad (1)$$

As a result, the voltage change at V_{out} due to this charge injection is given by equation,

$$\Delta V_{out} = \frac{\Delta Q_{ch}}{C_h} = -\frac{kWLC_{ox}}{C_h}(V_{DD} - V_{th} - V_{in}) \quad (2)$$

Notice that ΔV_{out} is linearly related with V_{in} and V_{th}. However Vth is nonlinearly related with V_{in}, therefore charge injection introduces nonlinear signal dependent error into the S/H circuit.

Clock feed through is occurring due to the gate-to-source overlap capacitance of the MOS switch, the voltage change at V_{out} due to the clock feed through is given by equation,

$$\Delta V_{out} = -C_{para}\left(\frac{V_{DD} - V_{SS}}{C_{para} + C_h}\right) \quad (3)$$

Where, C_{para} is the parasitic capacitance.

Charge injection and clock feed through are occurring due to intrinsic limitations of MOS transistor switches. Here, the charge injection and clock feed through errors are fixed by a bottom plate S/H circuit, and both of the errors are eliminated through a differential configuration.

In bottom plate circuit configuration, when both clk1 and clkd are high, the output of bottom plate Vob, tracks the input V_{in}. Then, clk1 goes from high to low first, therefore turning M5 and M6 off. At this time, the voltage at node A is zero and node B is at V_{in}. Since both drain and the source of M5 and M6 have a fixed potential, the charge injection caused by M5 and M6 when it turns off, is signal dependent and can be regarded as an offset error voltage. Next, clkd goes high to low, turning M1 and M2 off. The voltage drop, V_{AB} across the sampling capacitor, C_s, is now $-V_{in}$ plus and the channel charge is injected by M5 and M6. Disconnecting Cs from the input has the effect of isolating the input for the output. Although the charge injection due to the turning off of M1 and M2 is signal-dependent, the injection does not alter the charge stored on Cs. This is because node A is already left floating. Thus the voltage drop across Cs remains unaffected. By this analysis, S/H circuit suffers from a fixed charge injection error and a fixed clock feed through error.

In the circuit (fig 2), ck1 and ck2 are two non-overlapping clocks, and ckd1 is a slightly delayed version of ck1.when ck1 is high; V_{in} is sampled differentially onto the two capacitors (C_s). When ck2 is high, the op-amp operates in a unity-gain configuration and the op-amp output, V_{out}, will be equal to V_{in}. Thus the S/H circuit has a differential configuration and is used to eliminate both errors (clock feed through and charge injection).

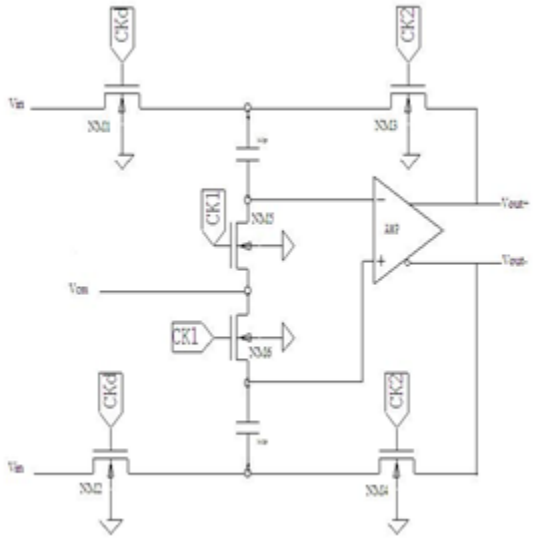

Fig (2): Fully differential sample-and-hold circuit.

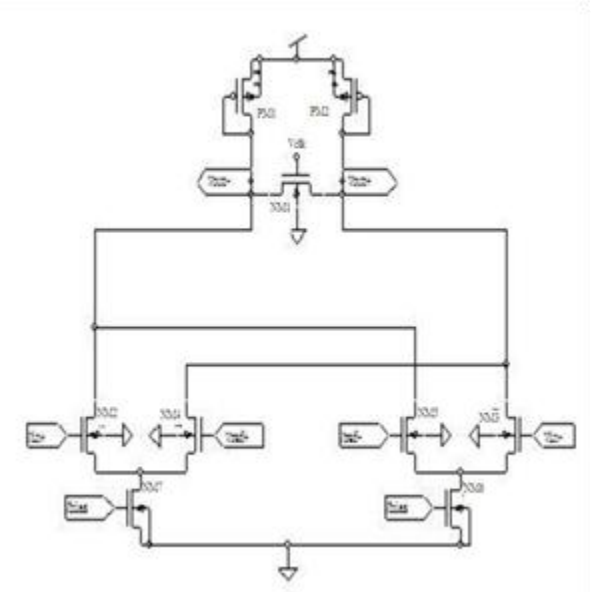

Fig (3): Preamplifier

2.2 PREAMPLIFIER

The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolates the input to the comparator [1]. The circuit diagram shown has four inputs, two are from differential S/H circuit and the others two are from the differential reference which is tapped off the resistor ladder. Figure 3 amplifies the differences of $V_{in+} - V_{ref+}$ and $V_{ref-} - V_{in-}$ respectively and then adds them together. A reset switch NM1 is connected between the two output nodes V_{out+} and V_{out-}. When the reset switch is turned on it erases the residual voltage from the previous sample. This happens during V_{clk} high period and S/H circuit in the track mode. When the reset switch is turned off, the V_{clk} is low and S/H circuit is in hold mode.

This noise is a direct result of the large amounts of charge which may be injected from the clocked comparators when switching from track to latch mode. The kickback noise is one of the most important problems in flash ADC because a bank of comparators shares the same input. The preamplifier is a fully differential preamplifier that deals with a kickback noise injected onto the pair of input nodes or onto the pair of reference as a common mode. The main function of preamplifier is to isolate the switching mode of the comparators from the input and reference nodes which reduce the impact of kickback noise. Choosing the device widths of the differential input transistors is a trade between the power consumption and bandwidth. As the transistor width increases the transistor trans-conductance (g_m) increases, gain bandwidth product increases, and the power consumption also increases.

2.3 LATCH AND TRACK COMPARATOR

The preamplifier gain is not enough to drive digital circuits, so we required increasing gain to track an analog input signal from comparator as follows. Here, the new latch and track based comparator is used to get a large gain. The circuit (Fig 4) is constructed by an input differential NMOS pair (NM1, NM2) and latch NMOS pair (NM3, NM4). The latch pair is equivalent to two cross coupled inverter. Here, one diode connected PMOS pair is used as a load, which separates the signal gain and common mode output voltage. When the circuit is in reset mode ie, clock is low, the differential output tracks the differential input. At this moment the switch NM5 is shorted to lower the first comparator voltage gain to less than one and erases memory of the previous decision. When the circuit is in latch mode ie, clock is high, the positive feedback is enabled and it generates the analog signal into full scale digital signal. As a result, the switch NM5 is used to get fast overdrive recovery which is a common problem for flash ADC. To overcome this problem it is important to include a reset switch between the comparator output nodes ie, on during the track phase. To speed up comparator operation it is important to reduce swing output ΔV and comparator gain which done through NM5. Otherwise the time constant becomes high which limits the speed, particularly in track mode,

$$\tau_{latch} = \frac{C_{tot}}{g_m} \ln\left(\frac{\Delta V}{\Delta V_O}\right) \quad (4)$$

Where, g_m→ Transconductance of field effect transistor,
C_{tot}→ Gate to source capacitance of field effect transistor,
ΔV→ Voltage difference between output voltages of the inverter, and
ΔV_0→ Initial voltage difference when the circuit is latching.

Here, high gain achieved by using latch and track technique rather than increasing number of gates.

2.4 GAIN COMPARATOR

The latch-track comparator has low gain, so it is required to increase the gain. Here, the latch and track comparator gain is increased by using gain comparator. Fig 5 shows the circuit of the comparator which is a single phase V_{clk}. It provides rail to rail output to the digital part of ADC. A fast reset scheme is introduced by resetting the output through two parallel discharge paths [1]. During the negative half cycle of the clock, the switching transistor M1 is turned on and the output discharged which forces the output ($V_{out+} - V_{out-}$) to be zero. During the positive half cycle of the clock, the switch is turned off which allows the comparator to evaluate its differential input and generate the corresponding differential output which is either $+V_{DD}$ or $-V_{DD}$. The input applied to the latch-track comparator is toggling from +LSB to –LSB and the outputs V_{op_comp1} and V_{on_comp1} are connected to the gain comparator. The stable digital output is produced by the gain comparator, proportional to the applied analog input signal.

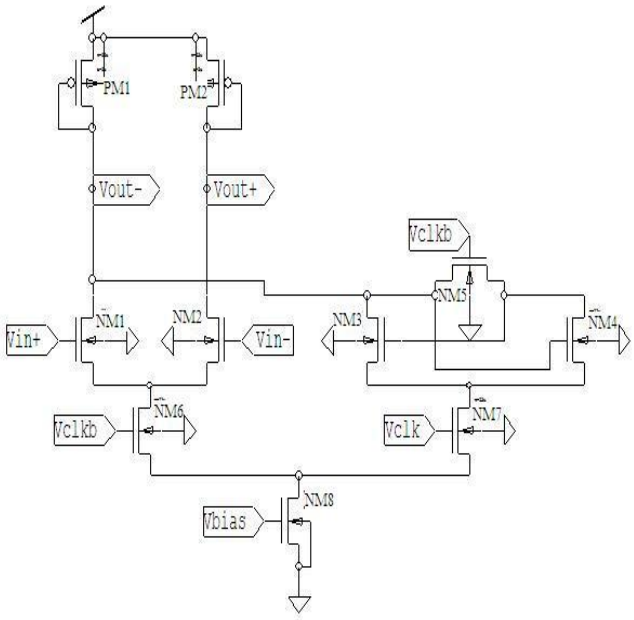

Fig (4): Latch-Track comparator

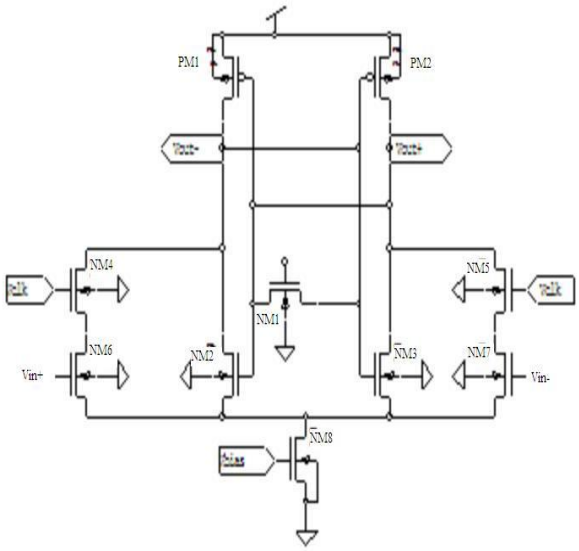

Fig (5): Gain Comparator

3 SIMULATION RESULTS

The proposed high speed low power flash ADC has been simulated with Tanner EDA using TSMC 0.18µm technology. The simulated results are obtained with the W/L ratio of 5µ/0.18µm for NMOS and 10µm/0.18µm for PMOS, which has been proved to be sufficient for ADC applications. The measured average power consumption of this proposed flash ADC is 5.3mW between a time of 2.5µsec, and output acquired with 1.8V supply voltage. From this proposed flash ADC, the measured maximum power dissipation is 6.4mW between a time of 0.1µsec, and the propagation delay is 0.62nsec. The power and delay values are verified using following formulas,

The average power consumption P for a time interval (t1, t2) is computed by using a trapezoidal rule approximation to evaluate the integral

$$P = \frac{1}{t_1 - t_2} \int_{t_1}^{t_2} P(\tau) d\tau \qquad (5)$$

Where,

$t_1 \rightarrow$ time at maximum power measured

$t_2 \rightarrow$ time at minimum power measured

Average propagation delay,

$$T_{pd} = \left(\frac{t_{pdr} + t_{pdf}}{2} \right) \qquad (6)$$

Where,

$t_{pdr} \rightarrow$ rising propagation delay (From input to rising output crossing VDD/2)

$t_{pdf} \rightarrow$ falling propagation delay (From input to falling output crossing VDD/2)

The simulated results are listed below; Figure (6a) shows an output response of sample and hold circuit. The output of sample and hold circuit is applied to the pre amplifier, to amplify the sampled signal before applying as an input to the comparator. The latch-track comparator accepts the input from pre amplifier ie, the output of pre amplifier considered as an input for comparator. The output response of latch-track comparator is shown in figure (6b). The output of latch-track comparator output gain is increased by using gain comparator. The response of gain comparator is shown in figure (6c). The flash ADC output is plotted in figure (6d). The layout of flash ADC structure is shown in figure (6e).

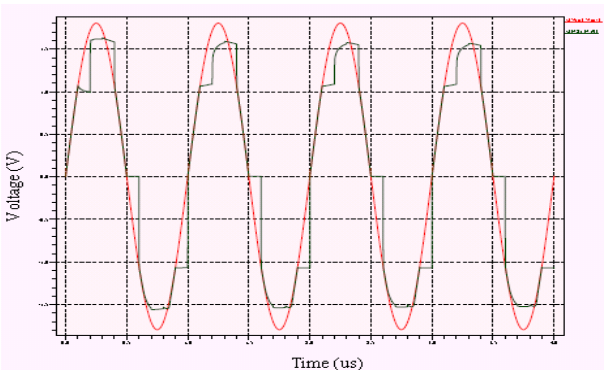

Fig 6a: Sample and hold

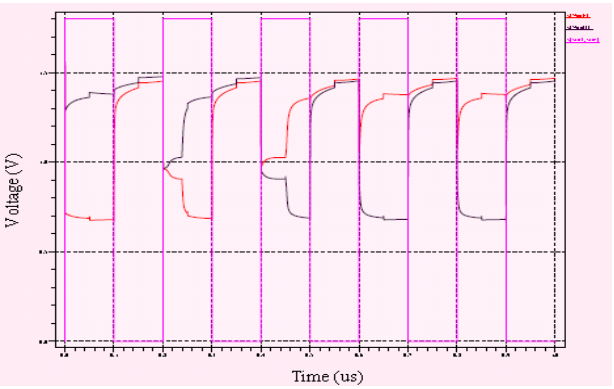

Fig (6b): Latch and track comparator

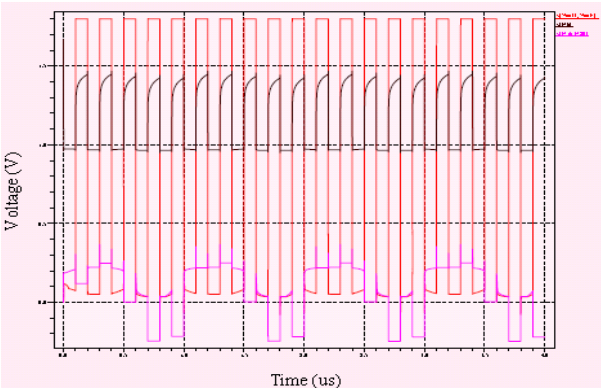

Fig (6c): Output of high gain comparator

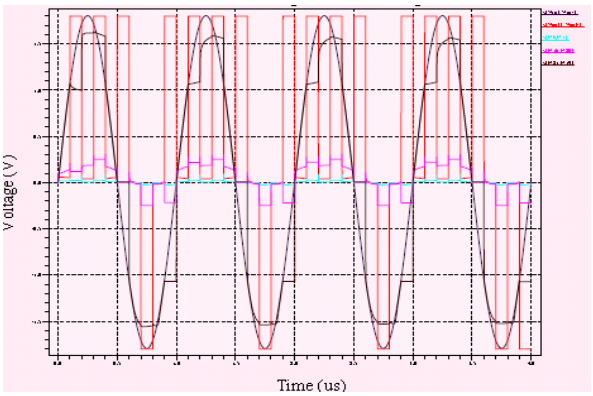

Fig (6d): Output of Flash ADC

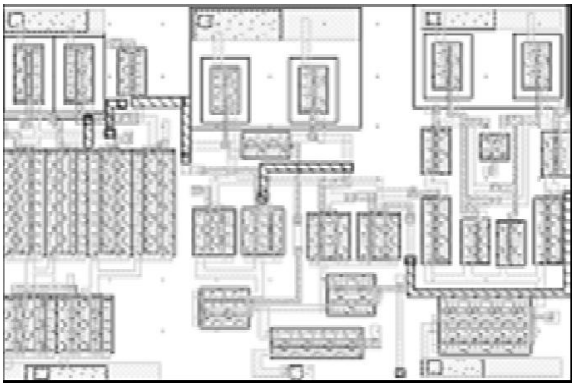
Fig (6e): Layout of Flash ADC

4 CONCLUSION

The proposed high speed low power flash ADC is designed and characterized which is suitable for ultra wide band (UWB) applications. It consists of sample and hold circuit followed by 2^n-1 number of preamplifier and latch-track comparator. The pipelined nature of the flash ADC allows the maximum operating frequency to be 1.2GHz. The proposed flash ADC design use a reduced layout area because it has less transistor dimensions and is a low power consumption device with 5.3mW at a time of 2.5μsec. Due to the less operating time and propagation delay, it produce a high performance. This high speed low power flash ADC is implemented using a 1.8v, 0.18μm CMOS technology.

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